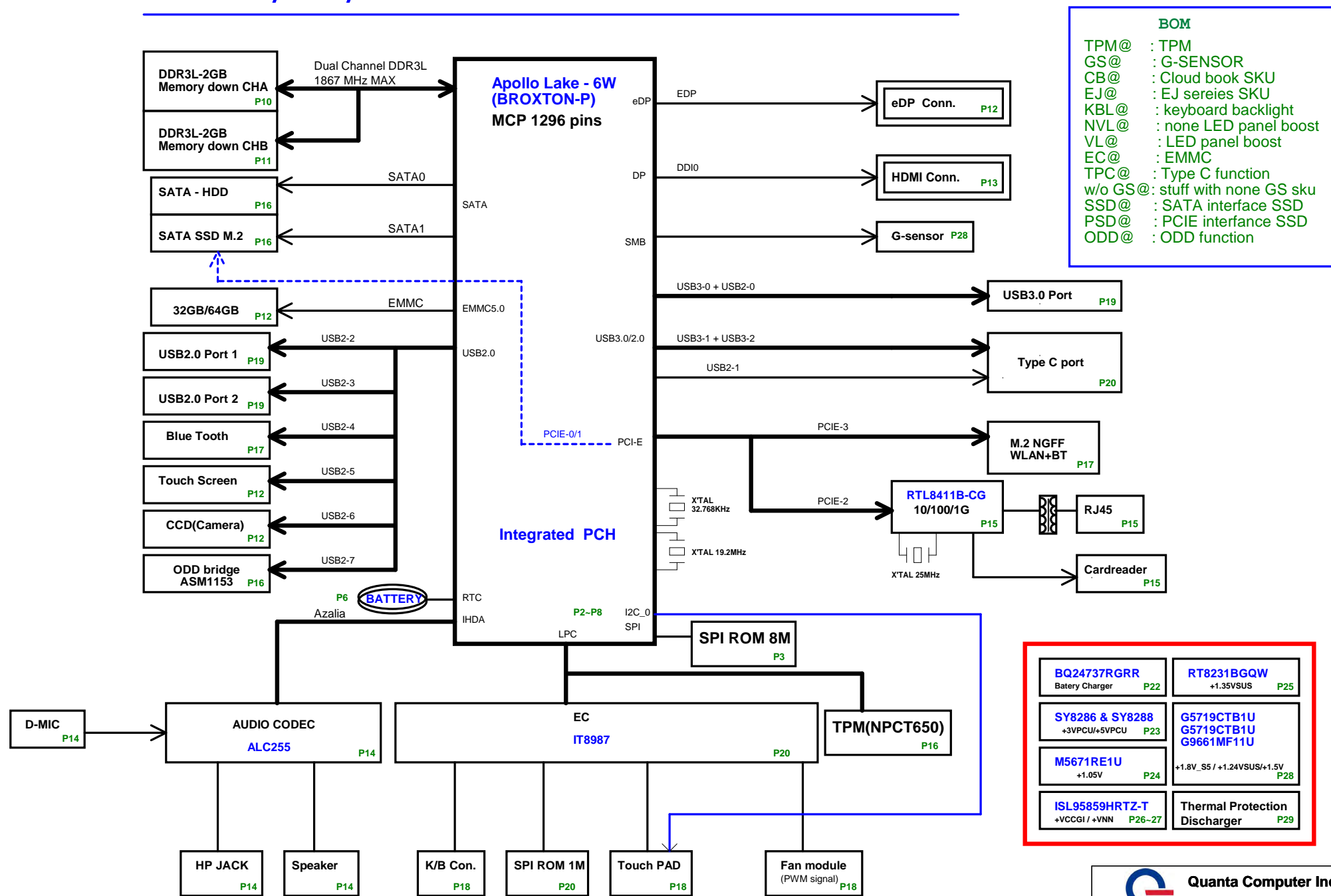
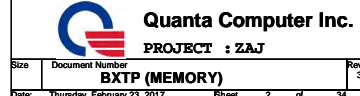
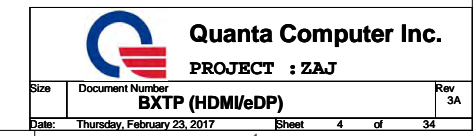


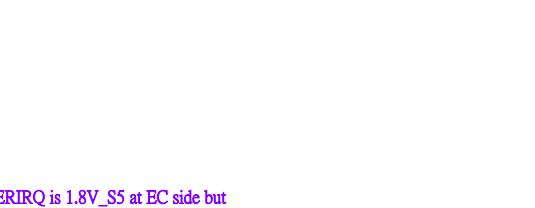
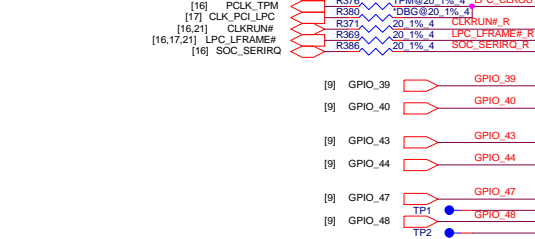
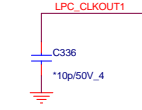
ZAJ/Z8P/Z8PA SYSTEM BLOCK DIAGRAM



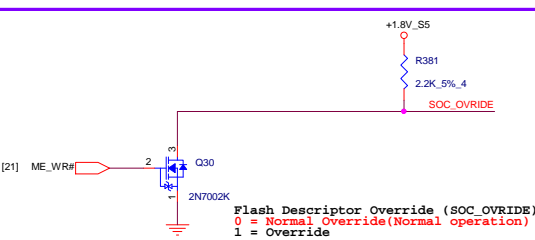
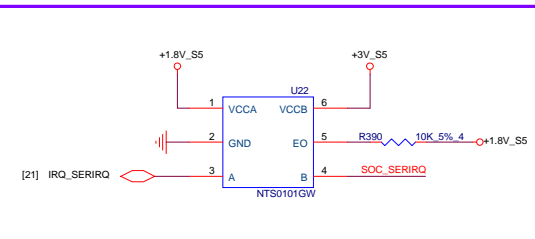




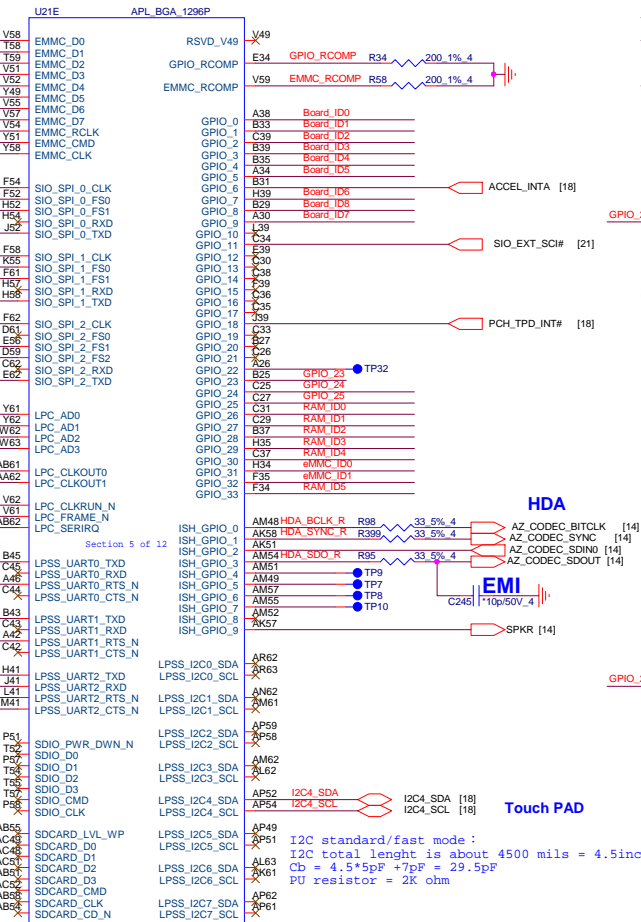
EMI



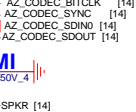
SERIRQ is 1.8V_S5 at EC side but 3V_S5 at CPU/TPM side



Flash Descriptor Override (SOC_OVRIDE)
0 = Normal Override(Normal operation)
1 = Override

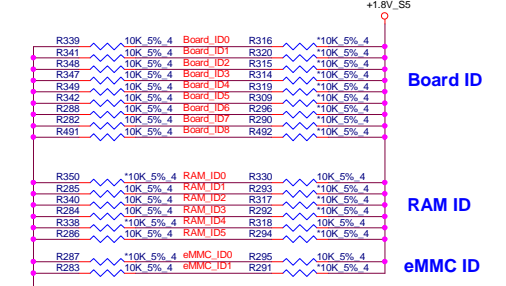
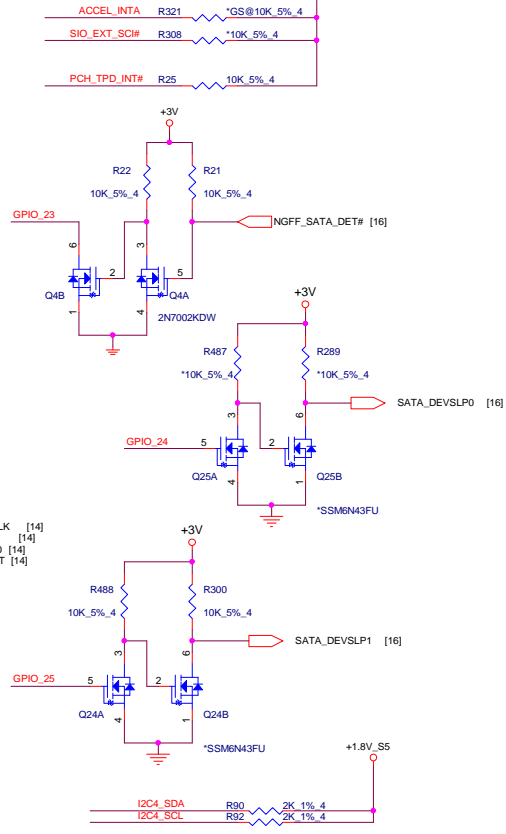


HDA



Touch PAD

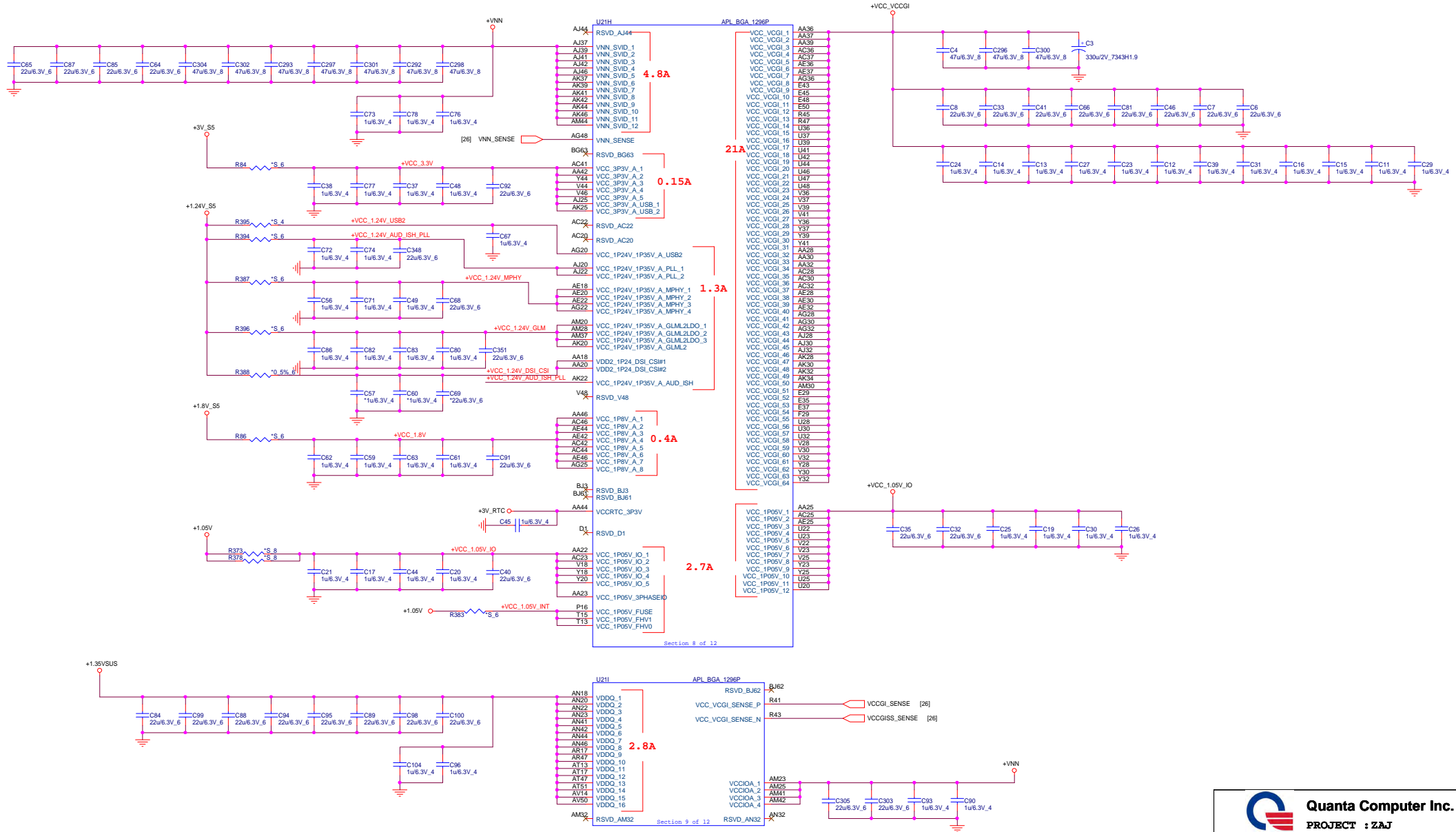
I2C standard/fast mode:
I2C total length is about 4500 mils = 4.5inches
Cb = 4.5*5pF + 7pF = 29.5pF
PU resistor = 2K ohm



RAM_ID5	RAM_ID4	RAM_ID3	Vender	Quanta PN	Description
0	0	0	Miron-2GB	AKD5J08TL08	IC: SDRAM(96P)MT41K256M16HA-125-E STNBSQ
0	0	1	Miron-2GB	AKD5908TL12	IC: SDRAM(96P)MT41K256M16TW-107-P STNBSQ
0	1	0	Hynix-2GB	AKD5P08W29	IC: SDRAM(96P)H5TC4063EPR-PB(A) STNBSQ
0	1	1	Samung-2GB	AKD5J00T5D4	IC: SDRAM(96P)K4B4G1646E-BYK0(FBGA) STNBSQ

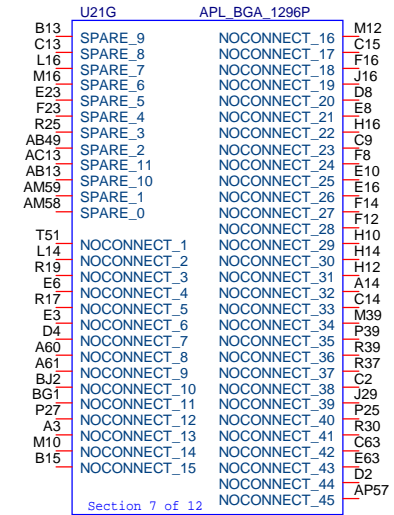
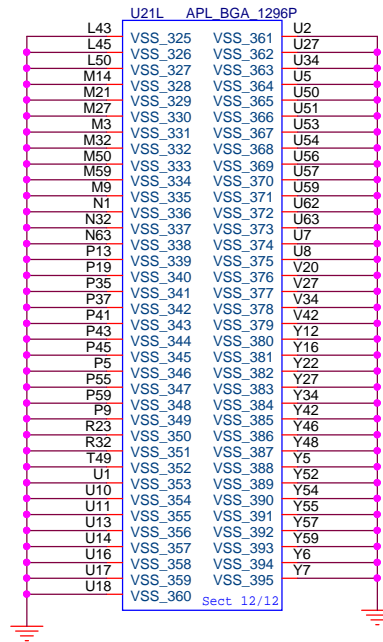
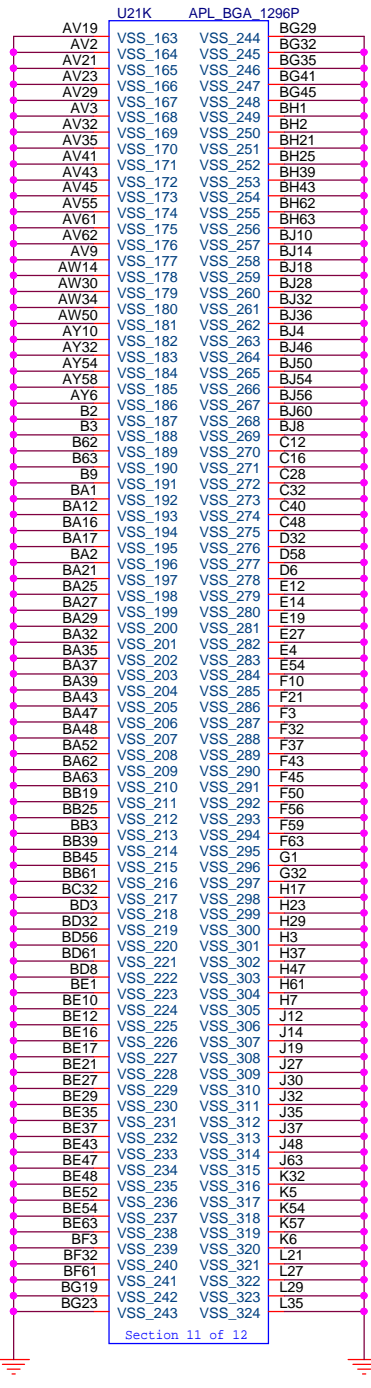
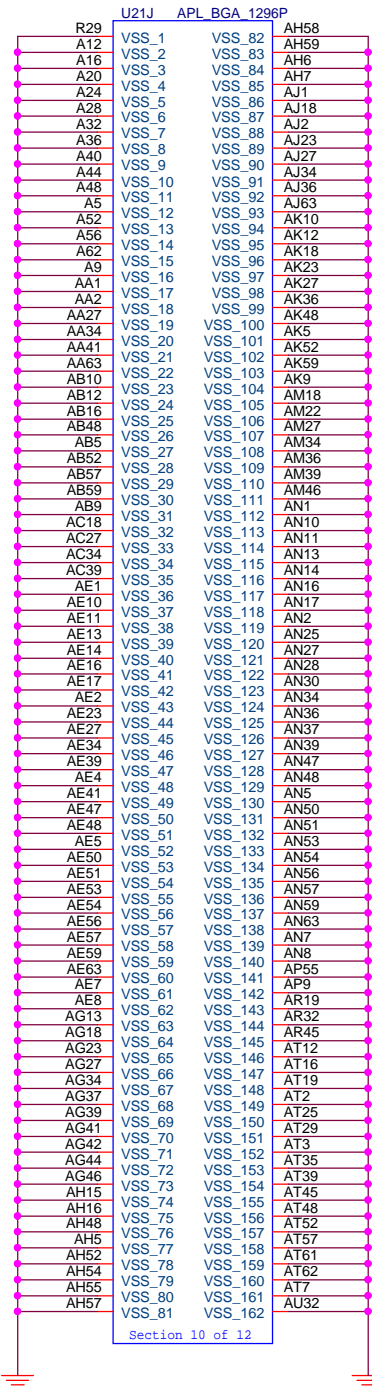
eMMC_ID1	eMMC_ID0	Vender
0	0	Samung 32/64GB
0	1	Hynix 32/64GB
1	0	Kingston 32/64GB

Quanta Computer Inc.
PROJECT : ZAJ
BxTP (EMMC/LPC/SMB/ISH)
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Apollolake ULT (GND)

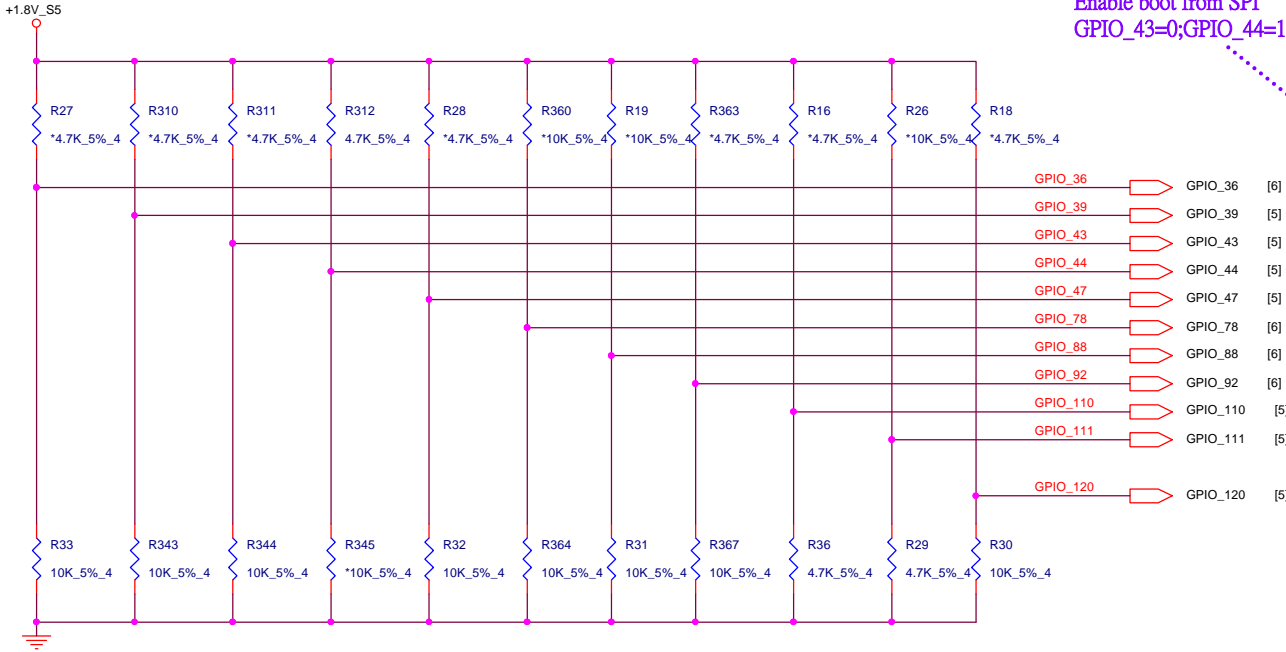
08



Quanta Computer Inc.
PROJECT : ZAJ

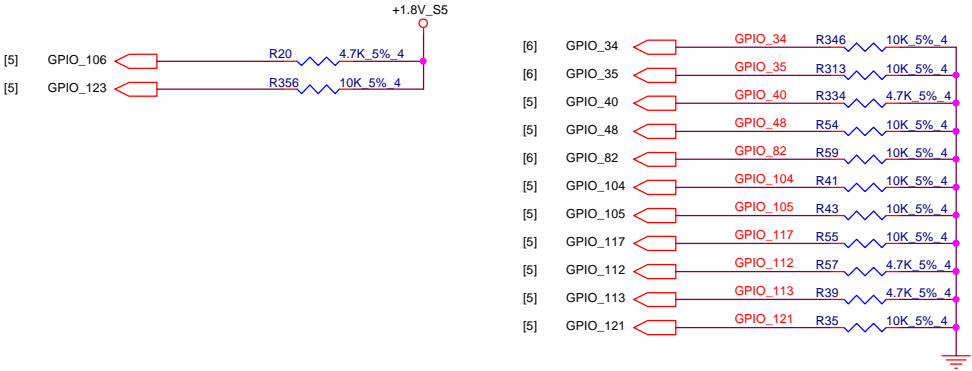
Size	Document Number	Rev
	BXTP (GND)	3A
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HARDWARE STRAPS



Follw APL WoW36 :
Enable boot from SPI
GPIO_43=0;GPIO_44=1

Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = Disable 1 = Enable



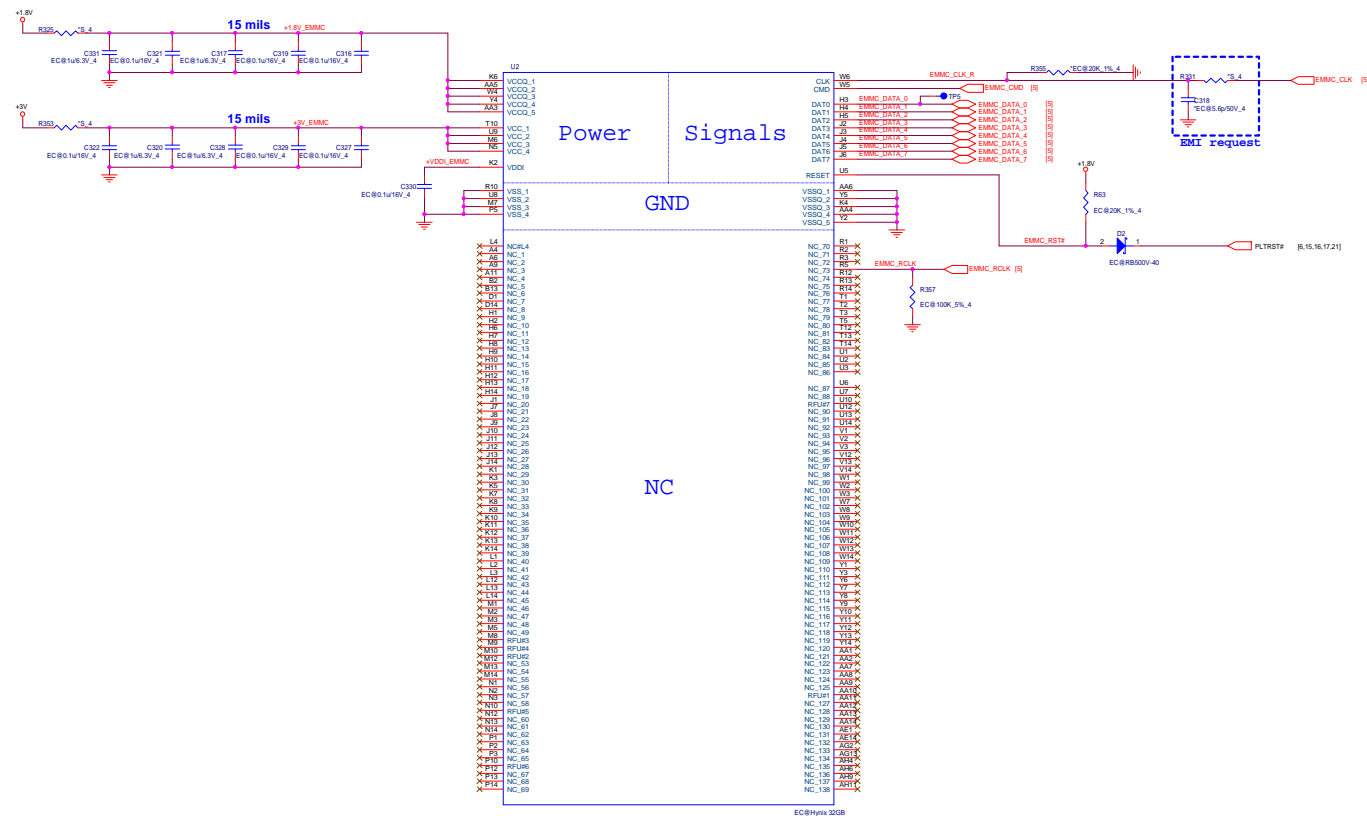


Quanta Computer Inc.
PROJECT : ZAJ

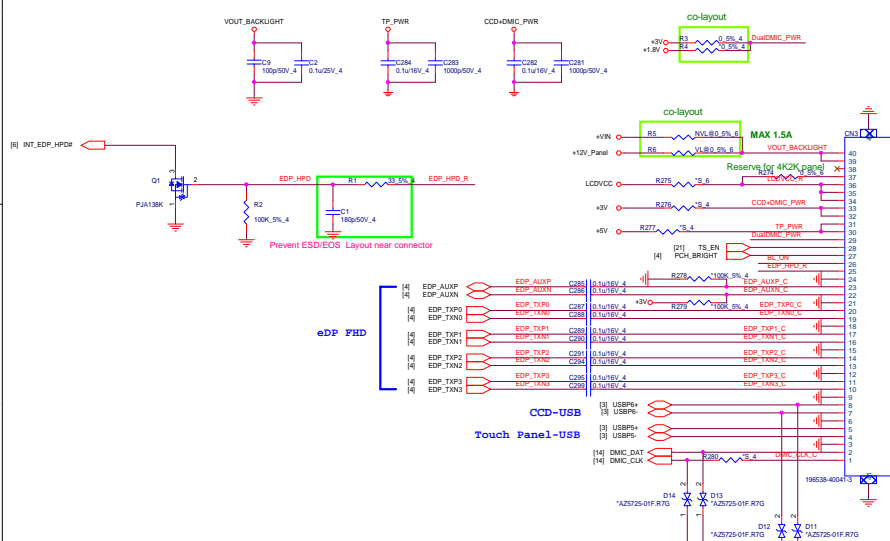
Size	Document Number	Rev
	HARDWARE STRAPS	3A
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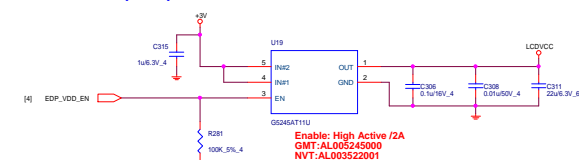




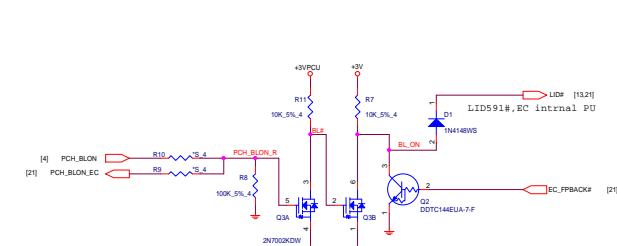
eDP CONNECTOR (LDS)



eDP Power (LDS)

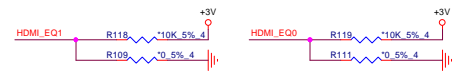
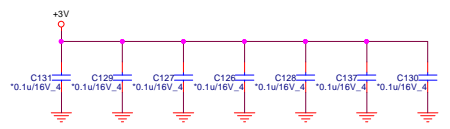


eDP Backlight (LDS)



HDMI (HDM)

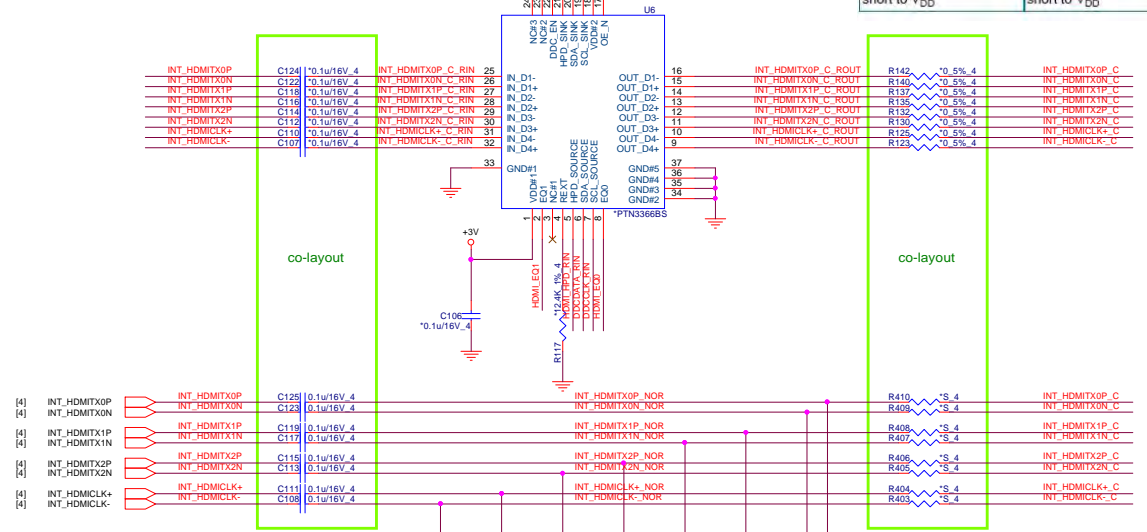
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

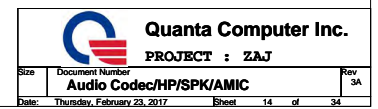


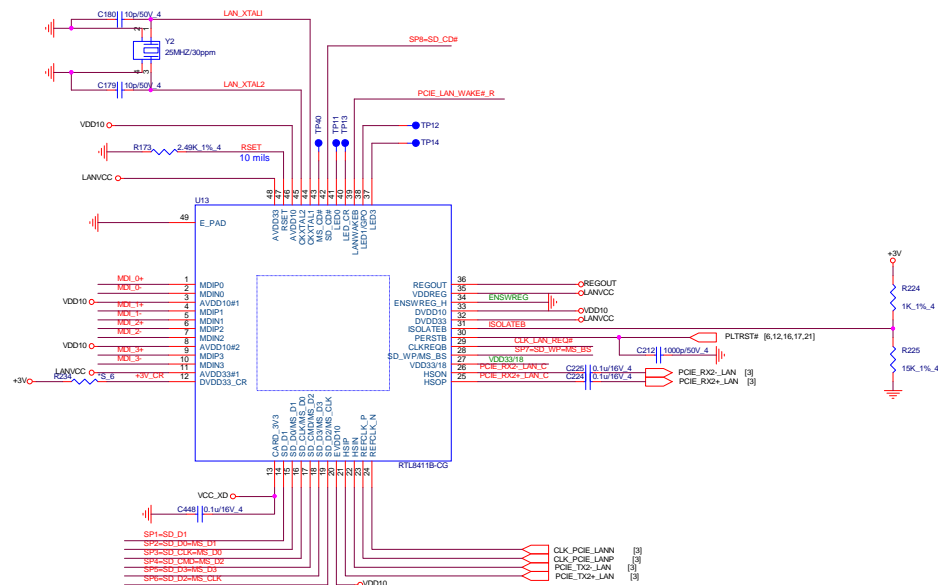
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

Table 5. Equalizer settings

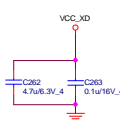
Inputs	EQ0	Equalization for 3 Gbit/s
EQ1 short to GND	short to GND	0 dB
EQ1 short to GND	short to V _{DD}	2 dB
EQ1 short to V _{DD}	short to GND	4 dB
EQ1 short to V _{DD}	short to V _{DD}	6 dB







SP1-SD_D1	C232	*10p/50V_4
SP2-SD_D0-MS_D1	C238	*10p/50V_4
SP4-SD_CMD-MS_D2	C445	*10p/50V_4
SP5-SD_D3-MS_D3	C446	*10p/50V_4
SP6-SD_D2-MS_CLK	C447	*10p/50V_4



EM

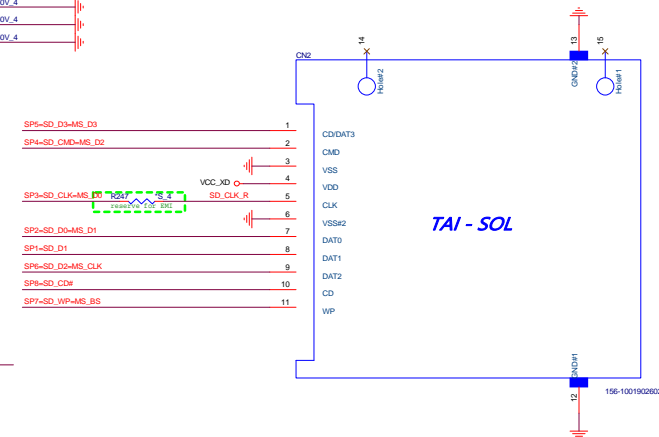
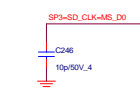
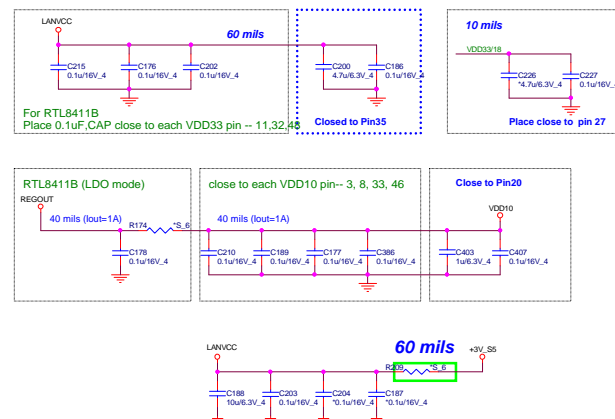


Figure 10 shows the LAN pin connections for the LAN8710. The diagram includes the following components and connections:

- Power Supply:** A 1.8V_S5 supply is connected to the LAN_VCC pin.
- Resistors:** Two 10K_5%_4 resistors are used. One is connected between LAN_VCC and POE_LAN_WAKES_R, and the other is connected between LAN_VCC and CLK_LAN_REQ.
- Signals:**
 - POE_LAN_WAKES# is connected to the POE_LAN_WAKES_R pin.
 - CLK_POE_LAN_REQ# is connected to the CLK_LAN_REQ pin.
- Transistors:** Two NPN transistors, Q15A and Q15B, are shown. Q15A's base is connected to POE_LAN_WAKES#, its emitter to ground, and its collector to the POE_LAN_WAKES_R pin. Q15B's base is connected to CLK_POE_LAN_REQ#, its emitter to ground, and its collector to the CLK_LAN_REQ pin.



The diagram shows the PCB layout for the N5682407 transformer. The transformer is represented by a blue square with pins 1 through 24. The layout includes the following components and connections:

- Capacitors:**
 - C10: 0.01uF, 50V, 4 (connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24).
 - C307: EJB1000P/3KV, 1808 (connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24).
- Transformer:** N5682407 (blue square).
- Pin Connections:**
 - Pin 1: LAN MCT0
 - Pin 2: LAN MCT1
 - Pin 3: LAN MCT2
 - Pin 4: LAN MCT3
 - Pin 5: LAN MCT4
 - Pin 6: LAN MCT5
 - Pin 7: LAN MCT6
 - Pin 8: LAN MCT7
 - Pin 9: LAN MCT8
 - Pin 10: LAN MCT9
 - Pin 11: LAN MCT10
 - Pin 12: LAN MCT11
 - Pin 13: LAN MCT12
 - Pin 14: LAN MCT13
 - Pin 15: LAN MCT14
 - Pin 16: LAN MCT15
 - Pin 17: LAN MCT16
 - Pin 18: LAN MCT17
 - Pin 19: LAN MCT18
 - Pin 20: LAN MCT19
 - Pin 21: LAN MCT20
 - Pin 22: LAN MCT21
 - Pin 23: LAN MCT22
 - Pin 24: LAN MCT23
- Layout Notes:**
 - Layout: All termination signal should have 30 mil trace
 - TF height limit = 4mm
 - TF height limit = 5.4mm

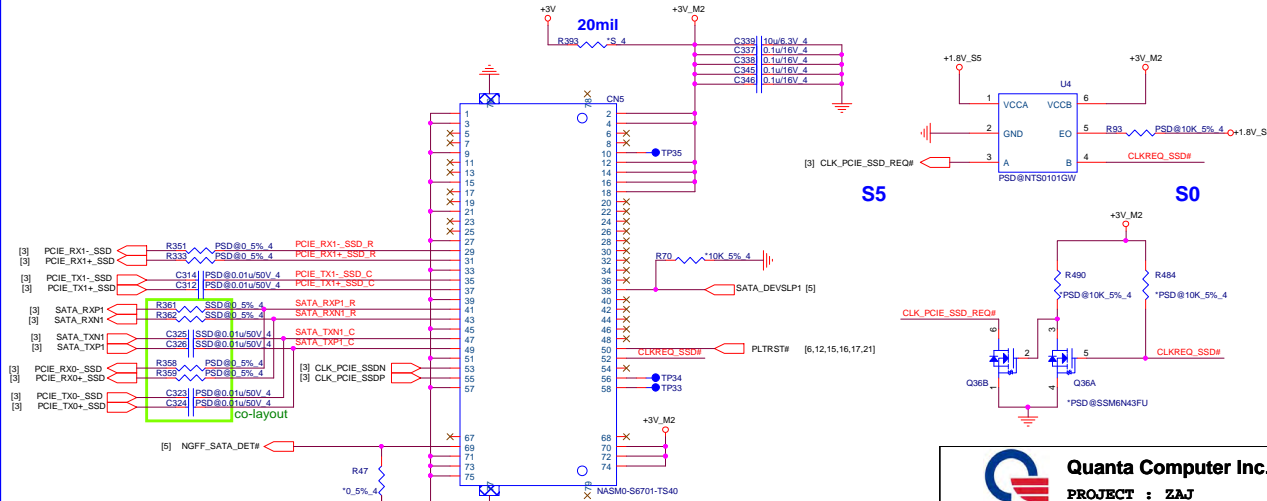
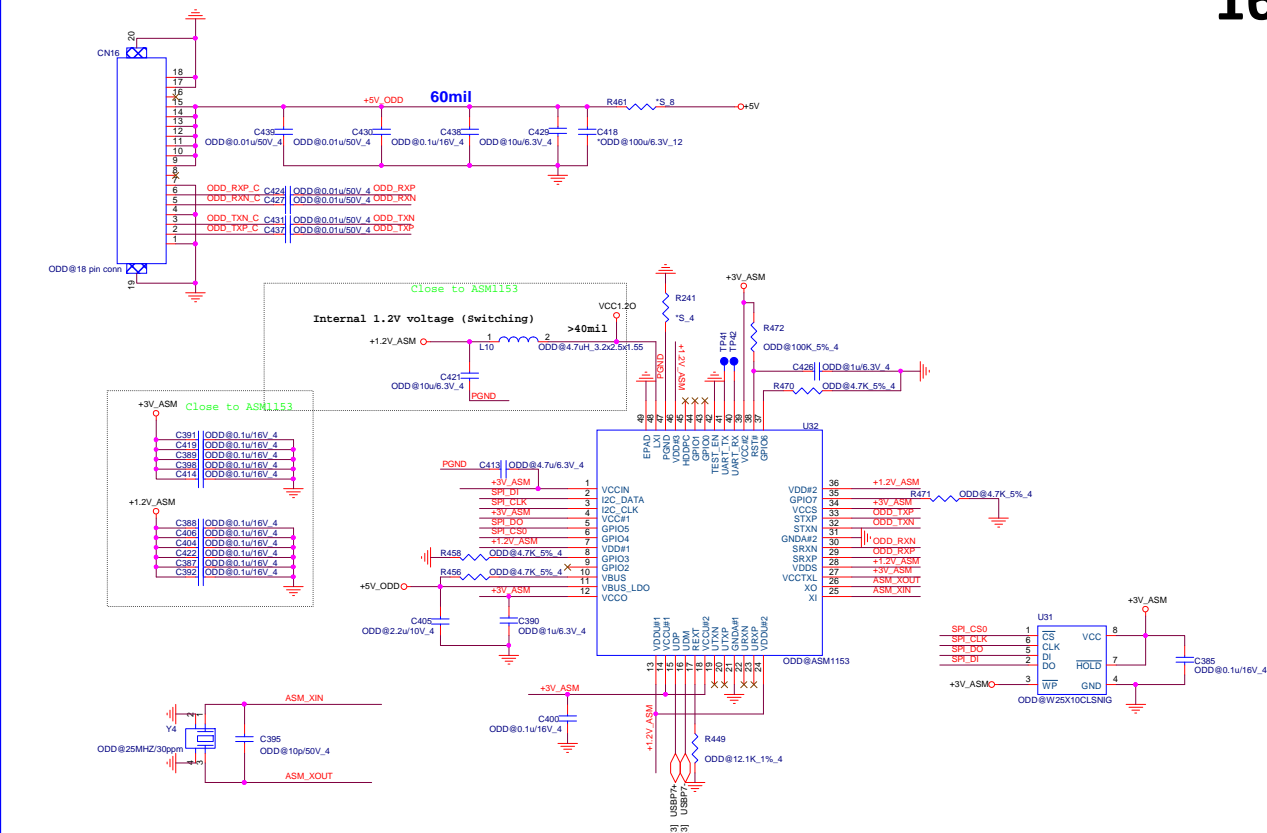
The diagram also includes a table of component values and a table of component descriptions.

SI	series	Vendor	Description
D08LL1LAN0	PCR	TRANSFORMER LLL LAN 24P (N0892407)	
D08SL1LAN1	PSK	TRANSFORMER SKL 10GA LAB (A-R3006)	
D08DL1LAN0	NOT	TRANSFORMER 20K LAN 24P (Q075009B 14P)	

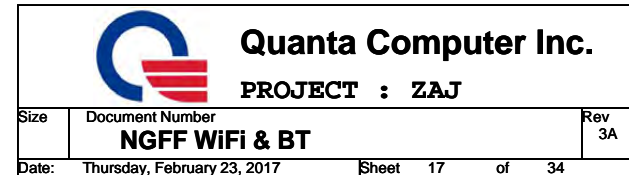
TF	height limit = 5.4mm	Vendor	Description
C10	0.01uF	50V	4
C307	EJB1000P/3KV	1808	



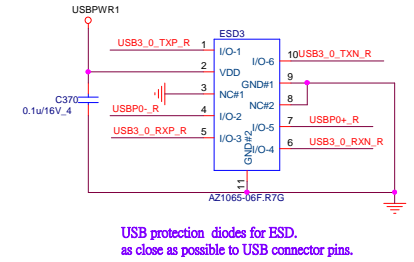
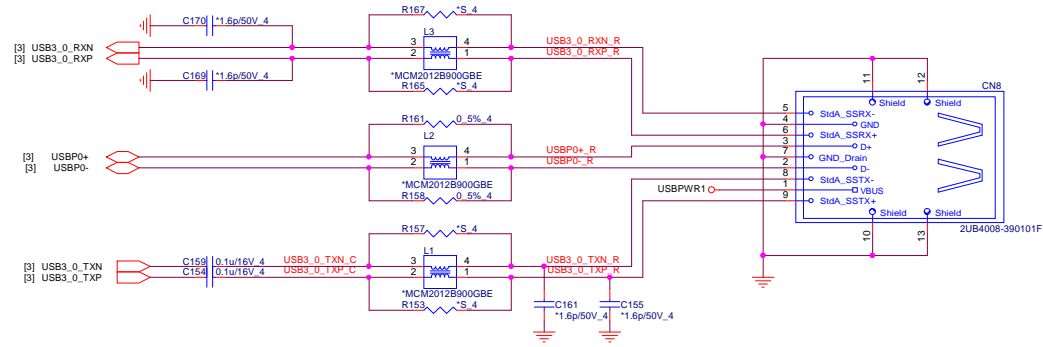
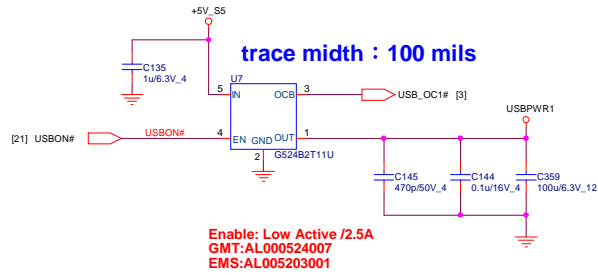
M.2 PCPIE & SATA SSD (NGF)



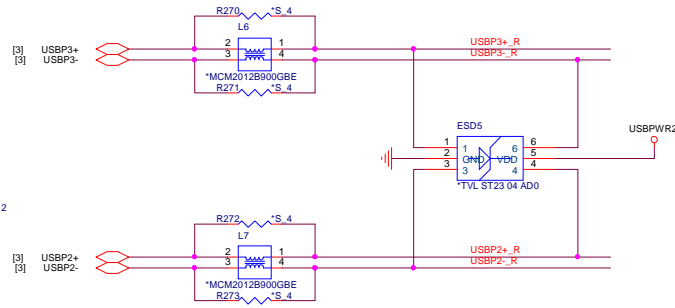
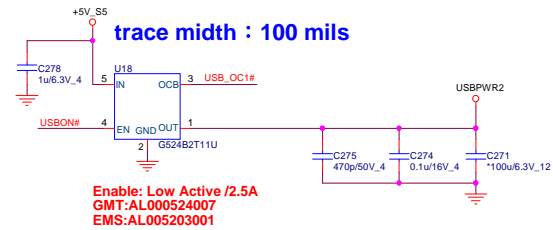
17



USB 3.0 (UB3)

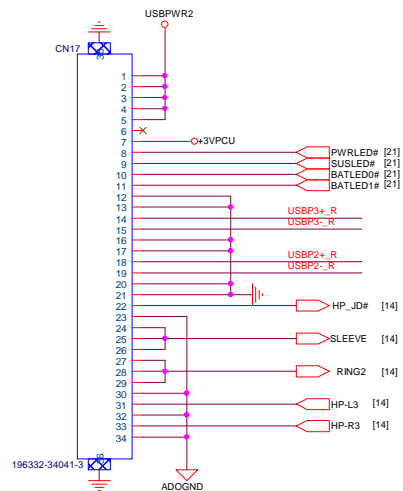


USB 2.0 (UB2)

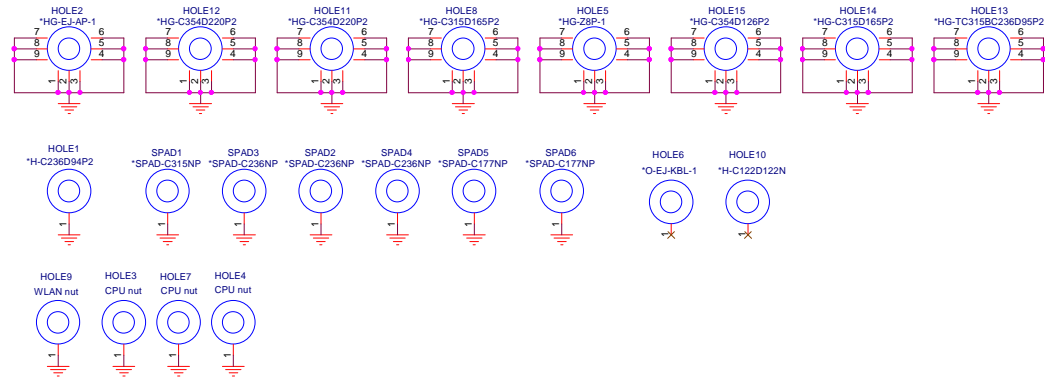


Stitch cap (EMC)

USB 2.0/LED/AUDIO JACK DB (UB2)



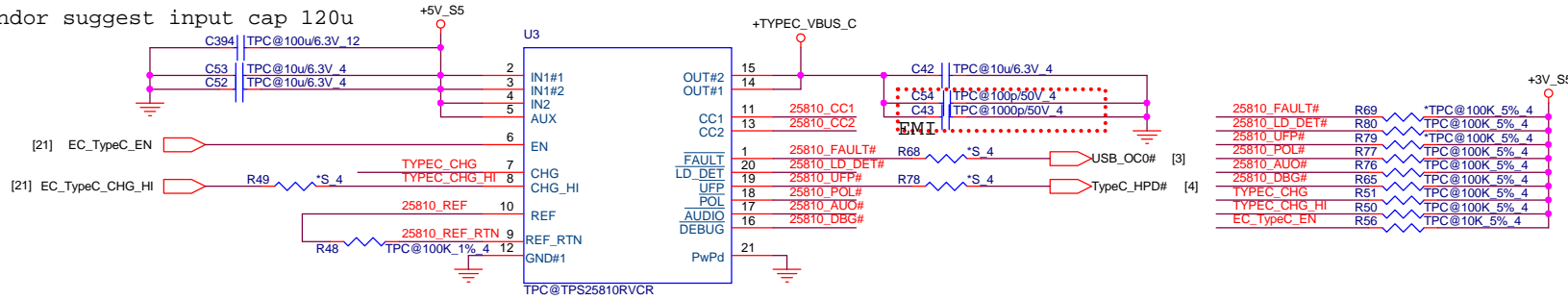
HOLE(OTH)



USB TYPE-C (UB3)

trace width : 150 mils

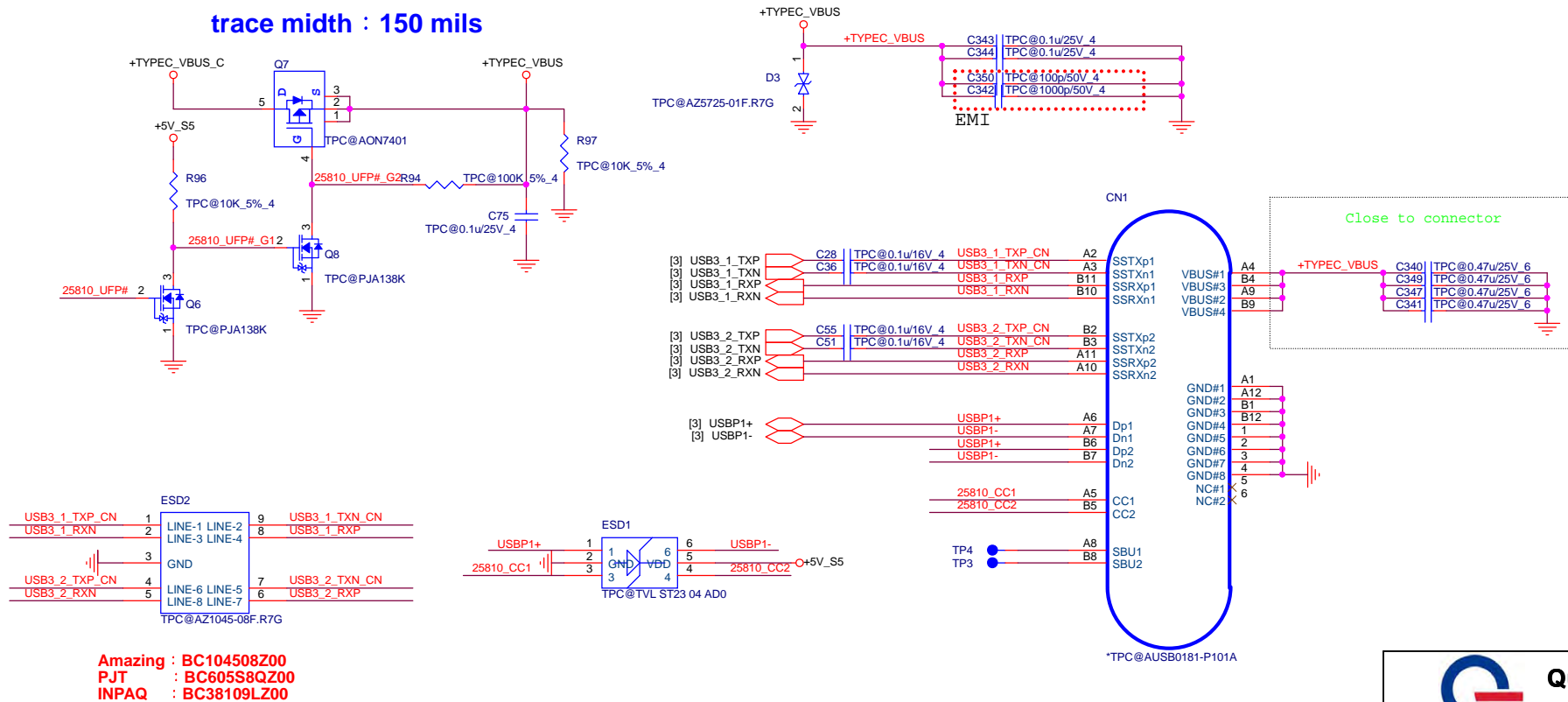
Vendor suggest input cap 120u



TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

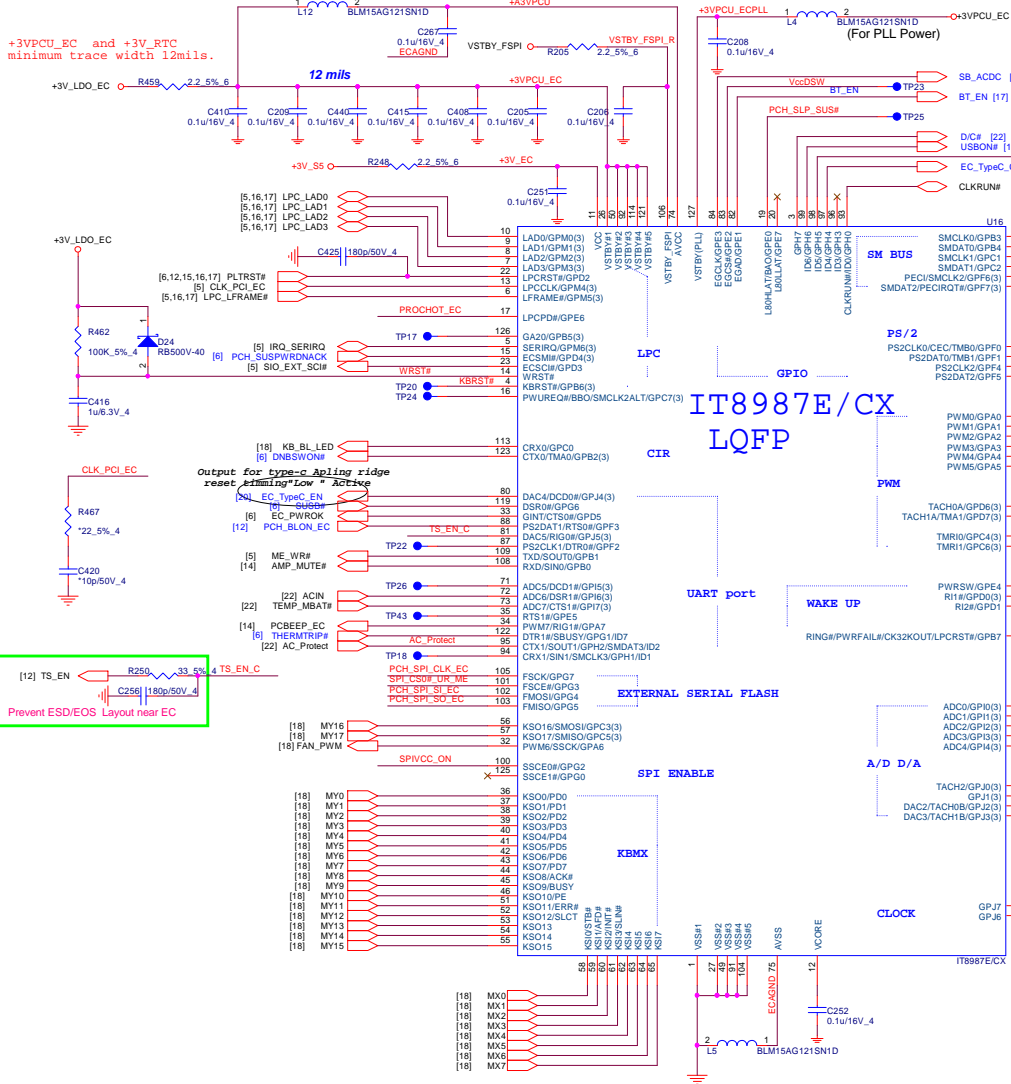
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

trace width : 150 mils



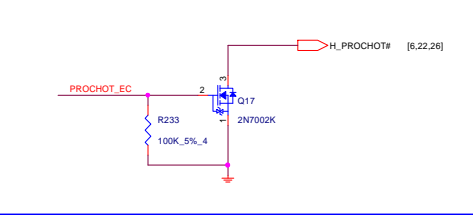
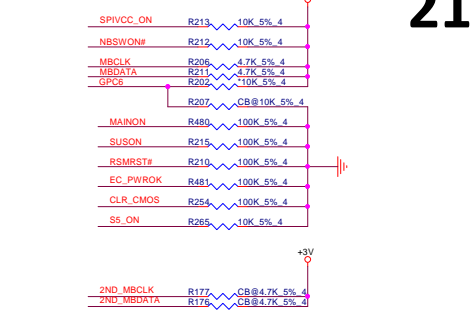
Amazing : BC104508Z00
PJT : BC605S8QZ00
INPAQ : BC38109LZ00

EC(KBC)

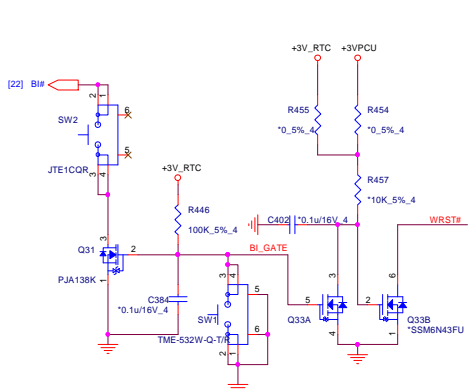


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PU/PD (KBC)



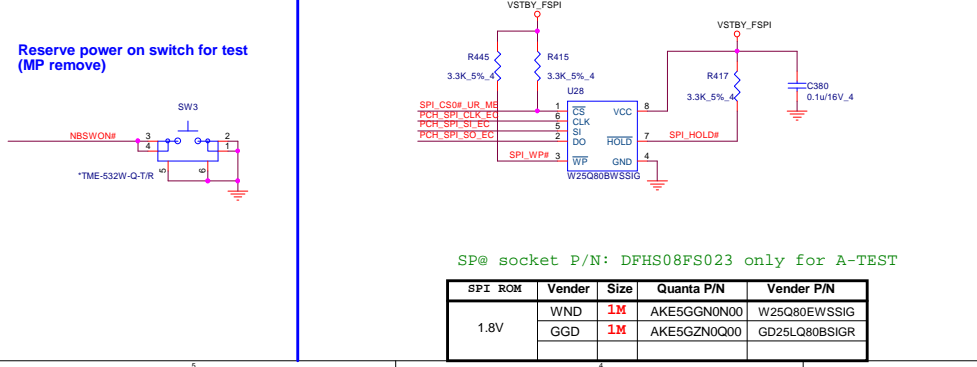
Battery Disable (FSW)



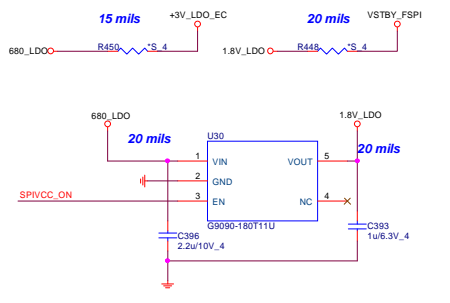
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	Thermal sensor
SM Bus 3	
SM Bus 4	

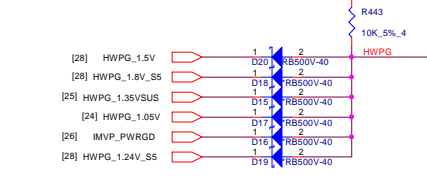
SPI ROM(KBC)



Power_Auto_Recovery



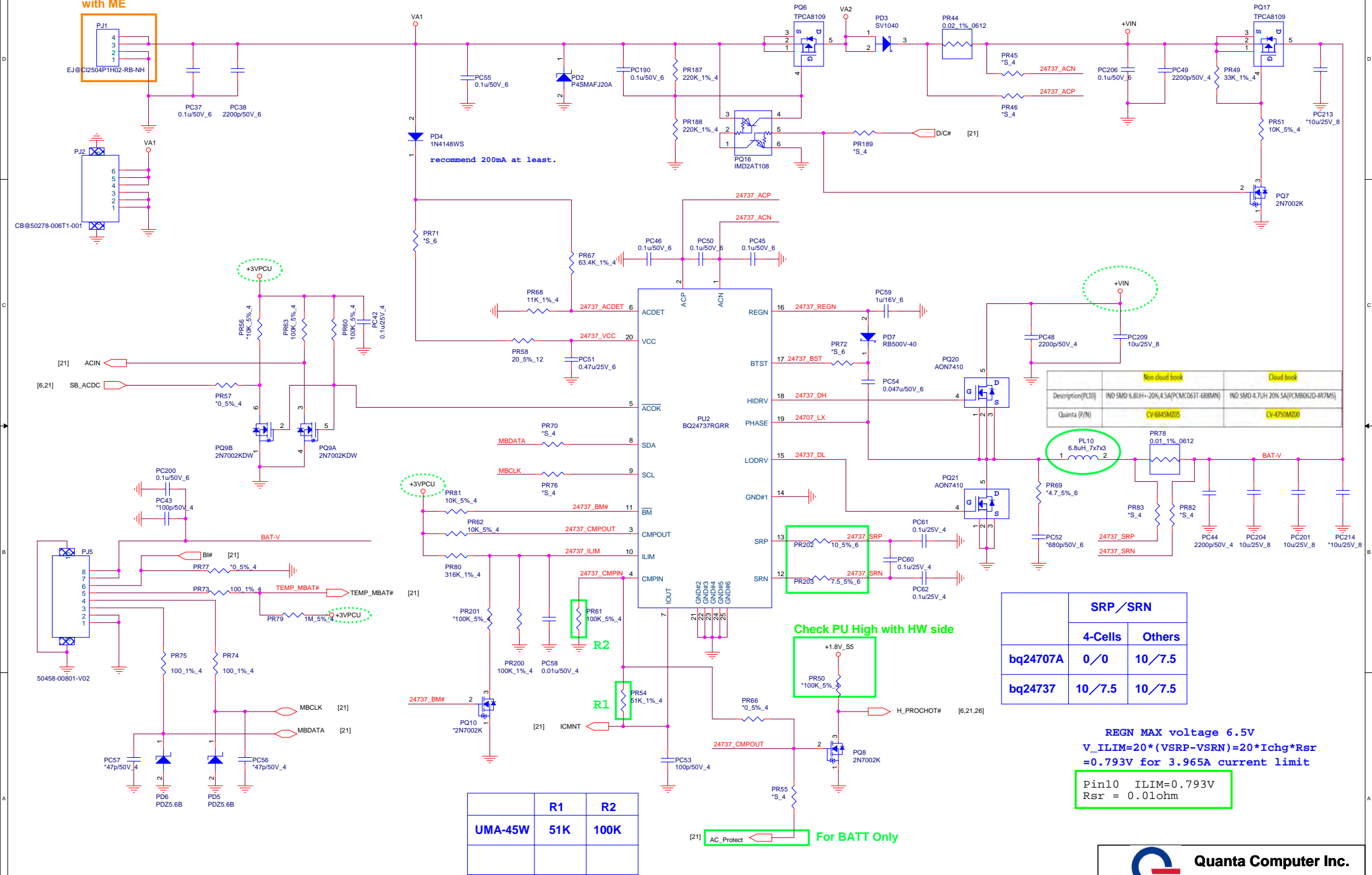
HWPG(KBC)



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Double Check ADP-IN Connector with ME



	Non cloud book	Cloud book
Description(PL10)	IND SMD 6.8uH ±20% 4.5A(PCM0637-68MM)	IND SMD 4.7uH 20% 5A(PCM0632-487MS)
Quanta (P/N)	CY4843M025	CY4750M020

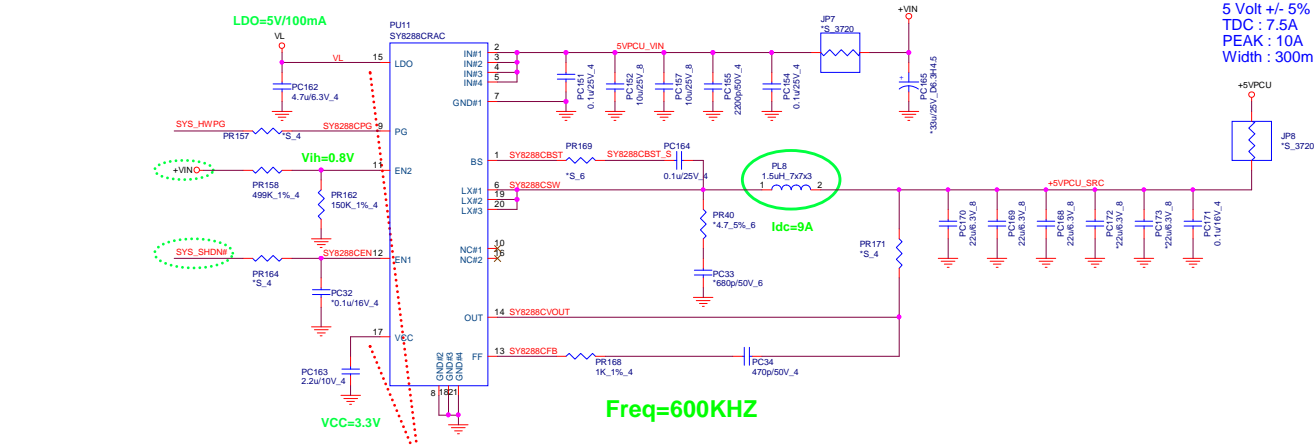
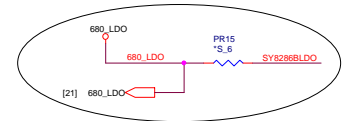
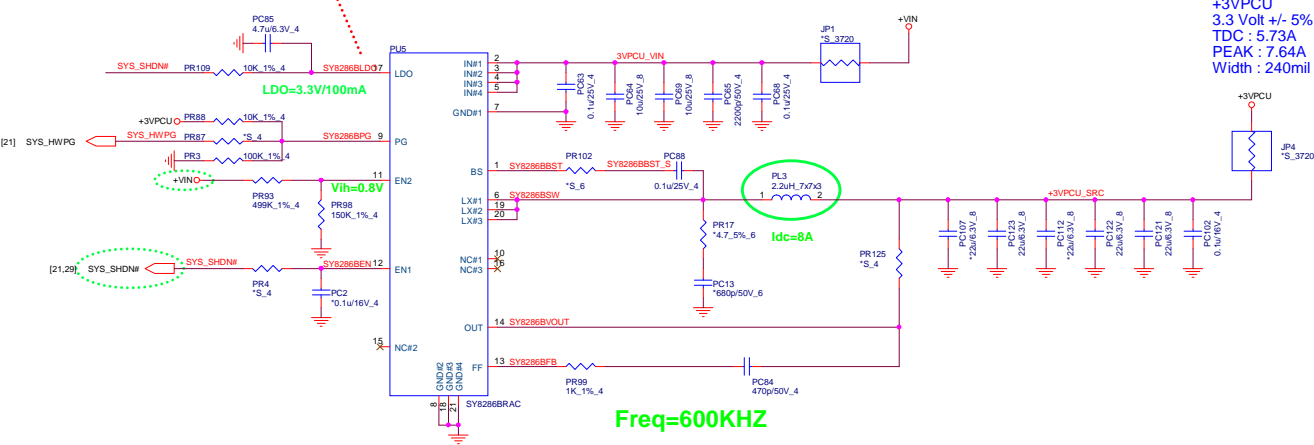
	SRP /SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (VSRP - VSRN) = 20 * Ichg * Rsr$
 $= 0.793V$ for 3.965A current limit

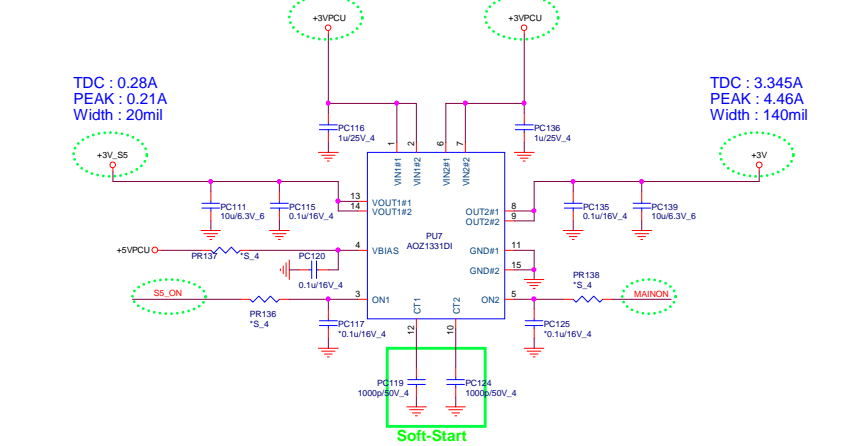
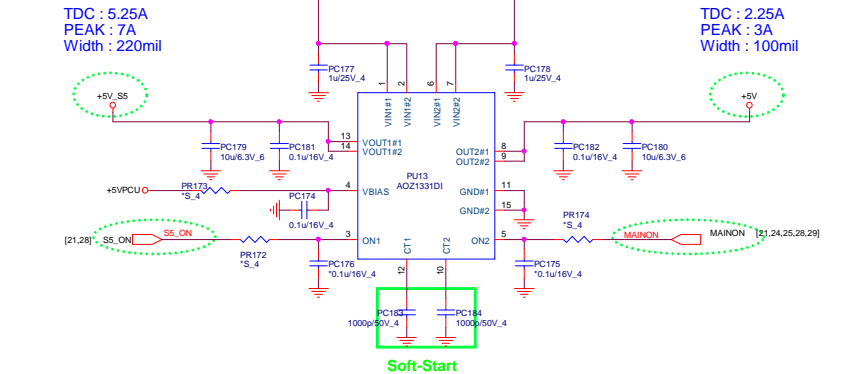
Pin10 ILIM=0.793V
 $Rsr = 0.01ohm$

	R1	R2
UMA-45W	51K	100K

Do Not add test pad on LDO pin



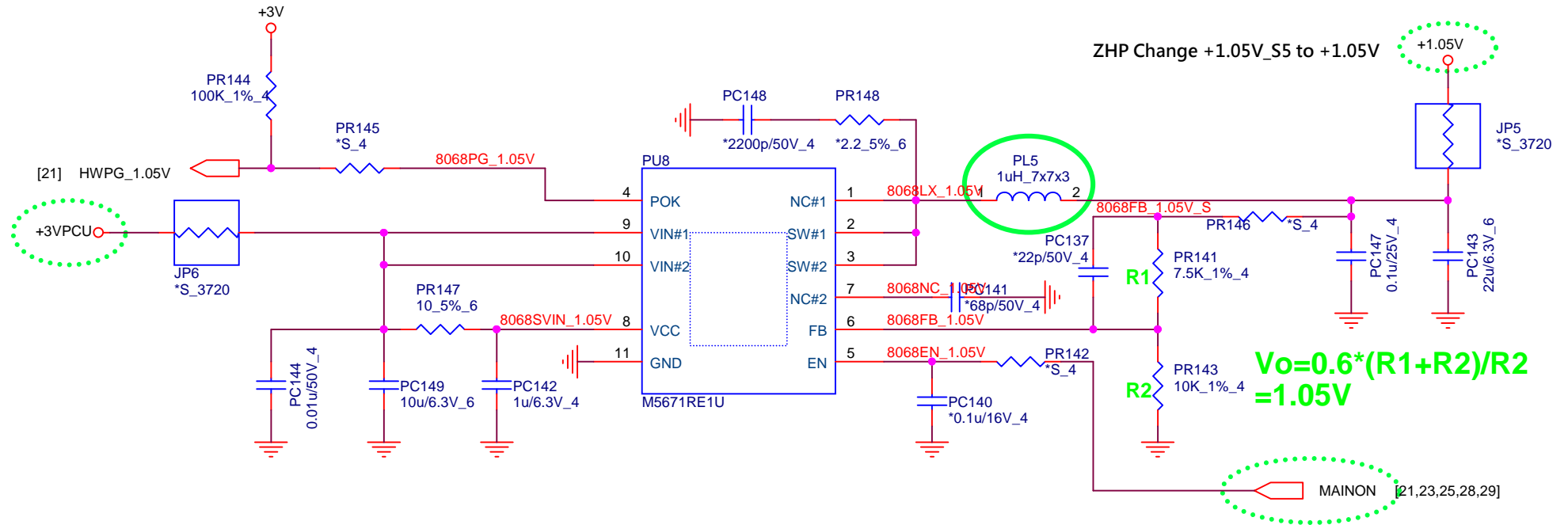
Do Not add test pad on VCC & LDO pin



[6,12,13,14,19,21,22,23,28] +3VPCU
 [6,7,26] +1.05V
 [4,5,6,12,13,14,15,16,17,18,21,23,25,26,28,29] +3V

+1.05V
 1.05Volt +/- 5%
 TDC : 2.025A
 PEAK : 2.7A
 Width : 100mil

ZHP Change +1.05V_S5 to +1.05V



$$V_o = 0.6 \cdot (R_1 + R_2) / R_2 = 1.05V$$

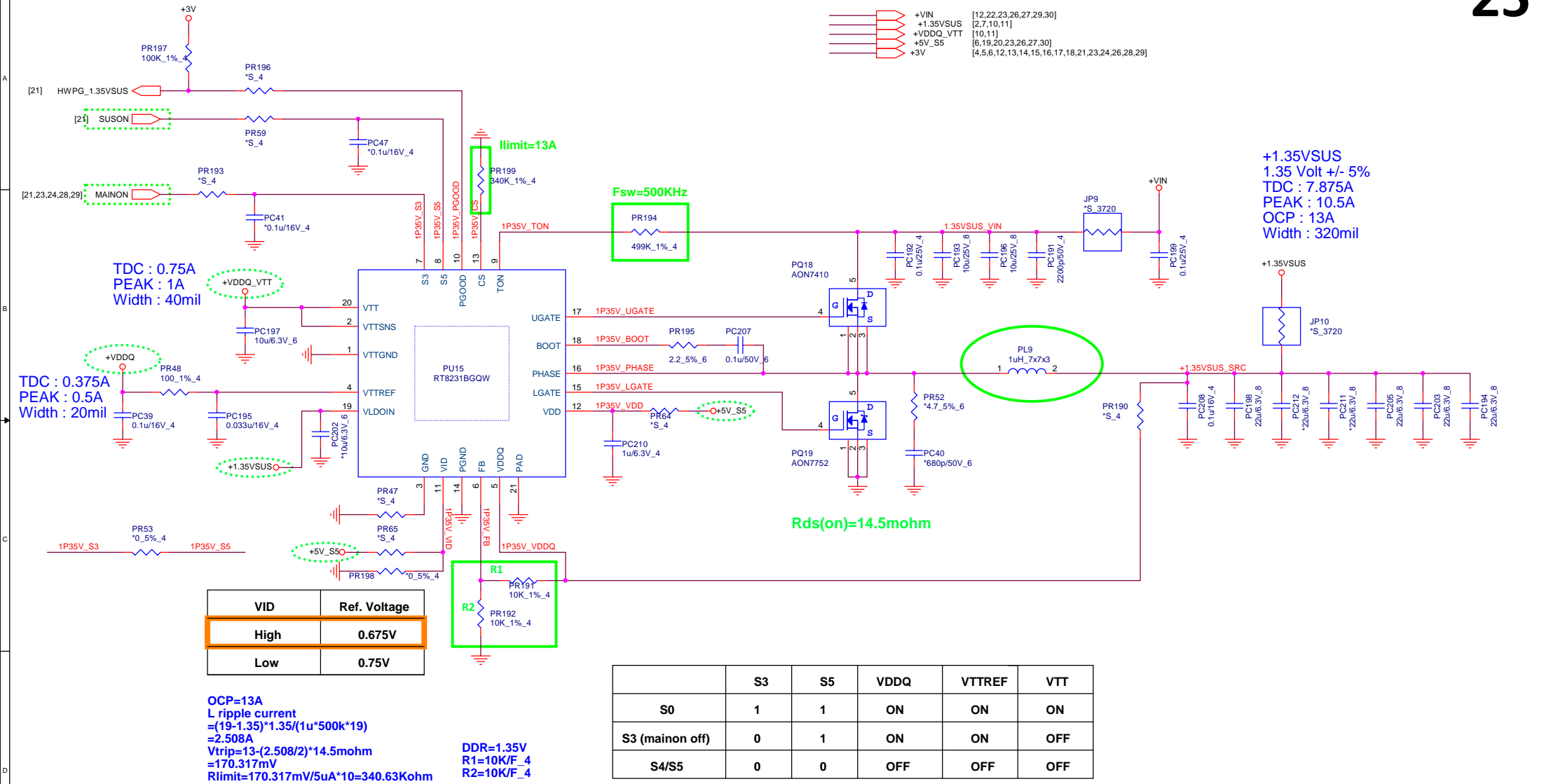


Quanta Computer Inc.

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Quanta Computer Inc.

PROJECT :

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	DDR3L (RT8231BGQW)	3A
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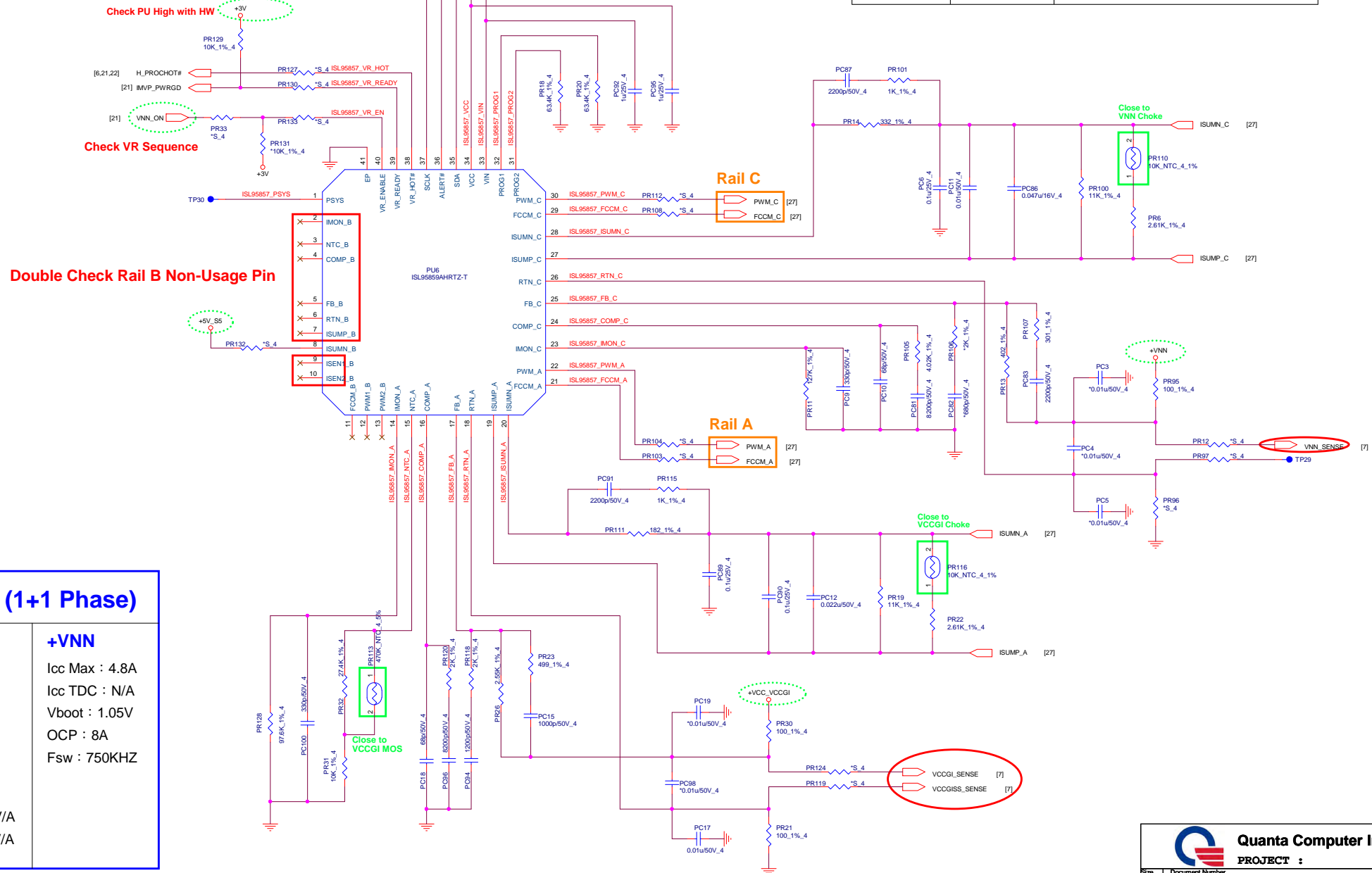
```
SVID_CLK   : UP:85 ohm   Series:95 ohm
SVID_ALERT : UP:68 ohm   Series:220 ohm
SVID_DATA  : UP:170 ohm  Series:20 ohm
```

IMVP8 VR Controller

Rail A (1 phase) : +VCCGI

Rail C (1 phase) : +VNN

Cloud book	P/N	Description
PR14	CS16342FB17	RES CHIP 634 (1/16W +-1%0402)
PC86	CH3226K1B00	CAP CHIP 0.022U 50V(+/-10%,X7R,0402)
PR111	CS12322FB09	RES CHIP 232 1/16W +-1%(0402)
PC90	CH3683K9B00	CAP CHIP 0.068U 16V(+/-10%,X5R,0402)



APL VR (1+1 Phase)

+VCCGI

Icc Max : 21A
Icc TDC : 18A
Vboot : 0V
OCP : 25A
Fsw : 750KHZ

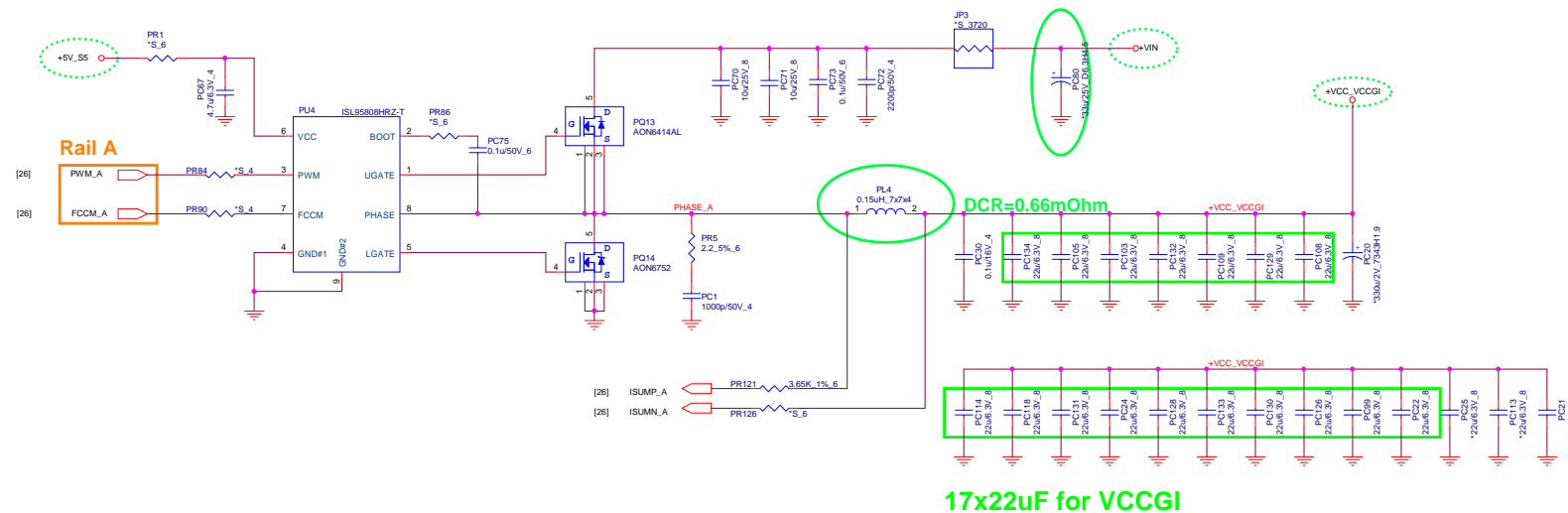
+VNN

Icc Max : 4.8A
Icc TDC : N/A
Vboot : 1.05V
OCP : 8A
Fsw : 750KHZ

VCCGI L/L :

R_DC_LL : 6mV/A
R_AC_LL : 6mV/A

VCCGI

**+VCCGI**

Icc Max : 21A

Icc TDC : 18A

Vboot : 0V

OCP : 25A

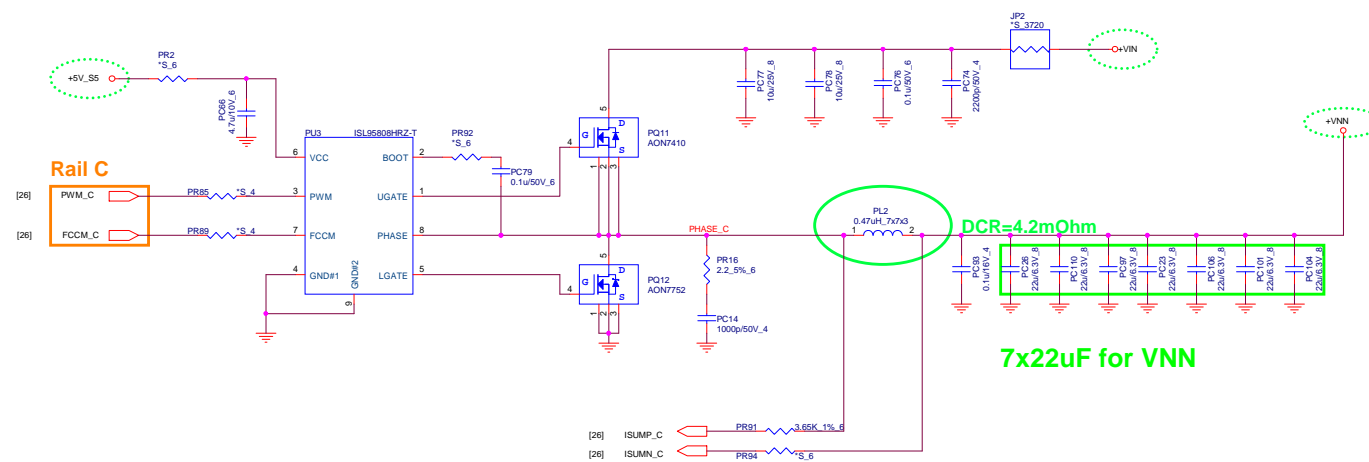
Fsw : 750KHZ

VCCGI L/L :

R_DC_LL : 6mV/A

R_AC_LL : 6mV/A

VNN

**+VNN**

Icc Max : 4.8A

Icc TDC : N/A

Vboot : 1.05V

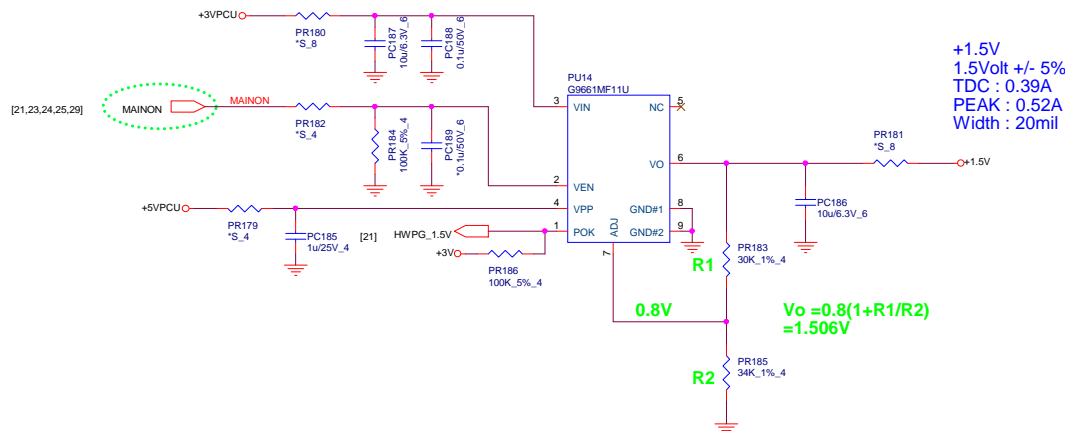
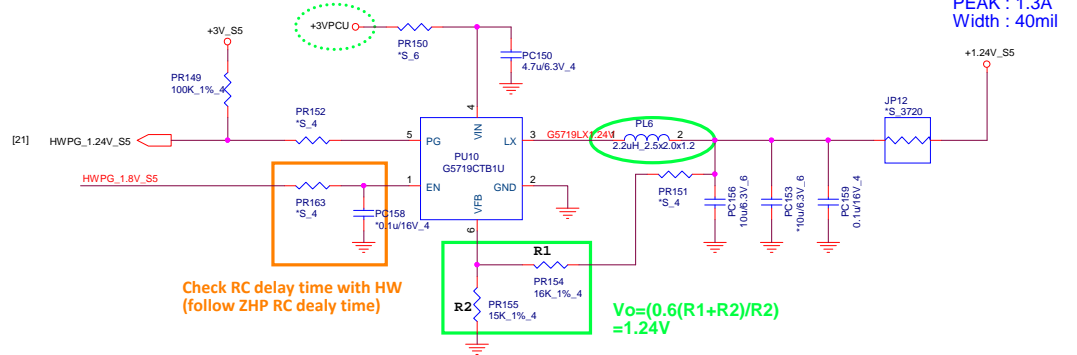
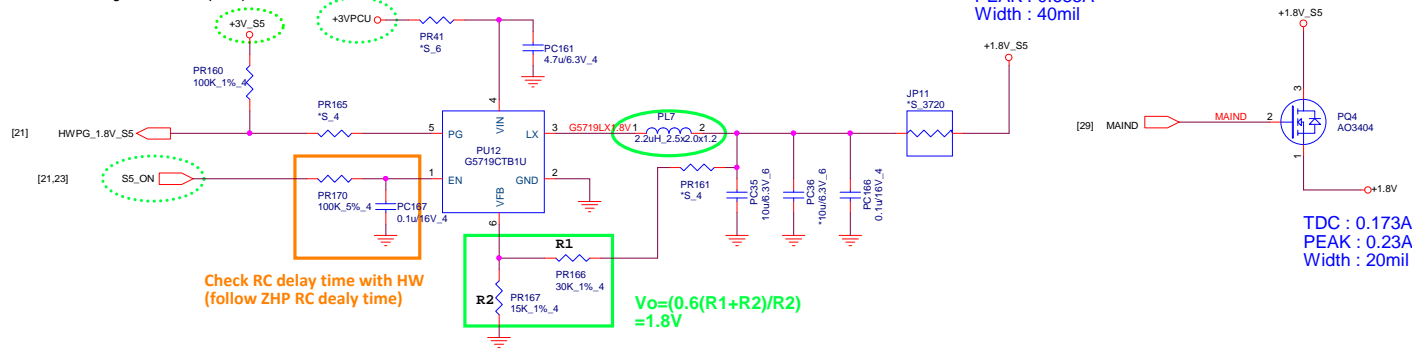
OCP : 8A

Fsw : 750KHZ

[6,12,13,14,19,21,22,23,24] +3VPCU
 [3,5,6,7,9,15,16,17,18,22] +1.8V_S5
 [7] +1.24V_S5
 [12,13,29] +1.8V
 [14] +1.5V

[5,6,7,15,16,18,20,21,23] +3V_S5
 [23] +5VPCU
 [4,5,6,12,13,14,15,16,17,18,21,23,24,25,26,29] +3V

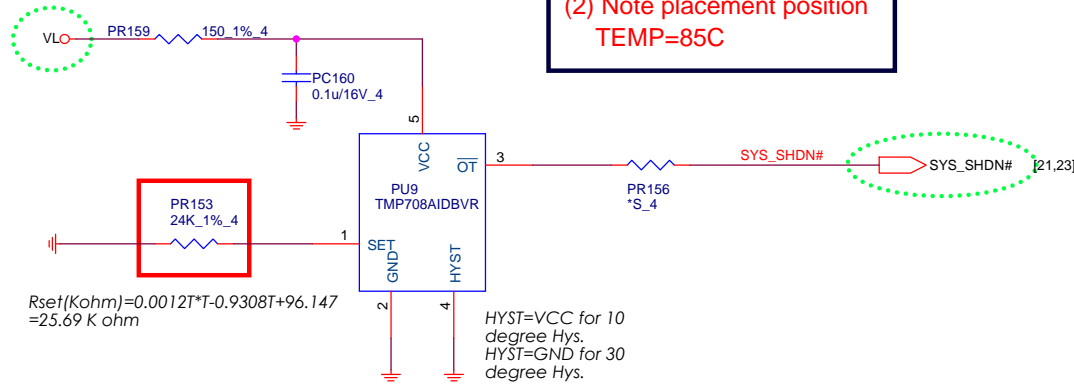
ZHP change +1.8V_S5 PG pull up to +3V_S5



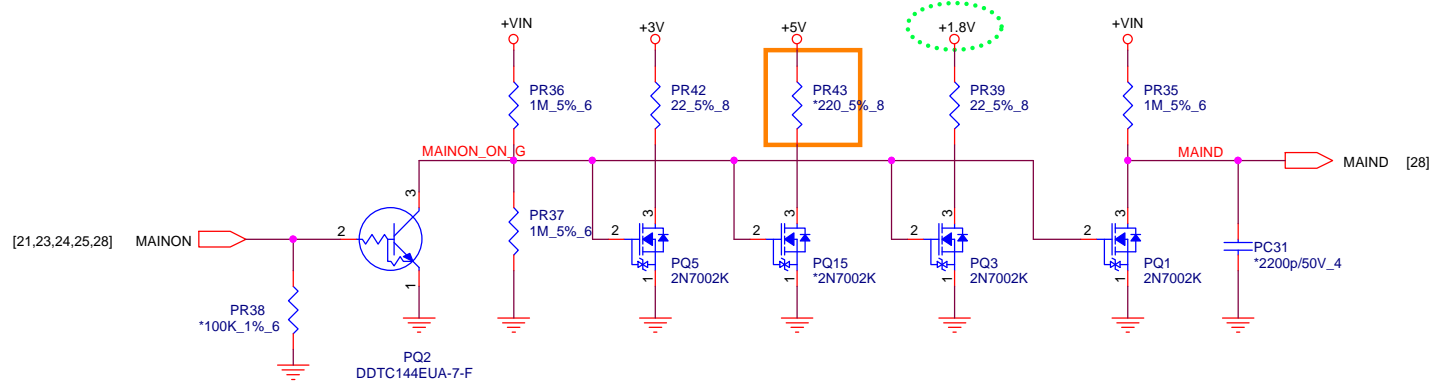
[23] VL
 [12,22,23,25,26,27,30] +VIN
 [4,5,6,12,13,14,15,16,17,18,21,23,24,25,26,28] +3V
 [12,13,14,16,18,23] +5V
 [12,13,28] +1.8V

Thermal Protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position TEMP=85C



+5V PU High R= 220 ohm for Bo-Bo sound issue.

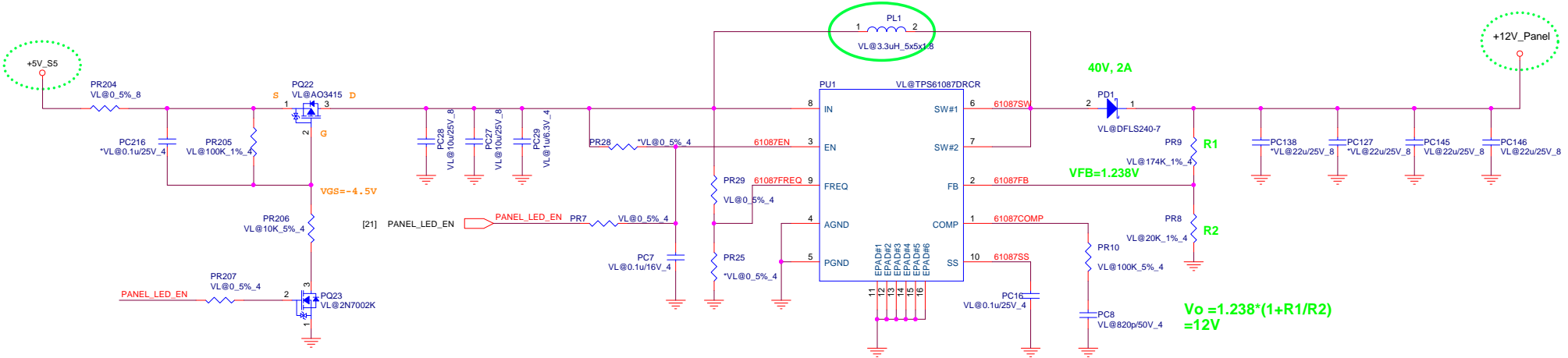


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PROJECT :

Panel Spec (TFT-LCD 14")
 VLED : 6V~21V (Typ:12V)
 Power Consumption : 3W (MAX)

+12V_Panel
 12 Volt +/- 5%
 PEAK : 0.35A
 Width : 20mil

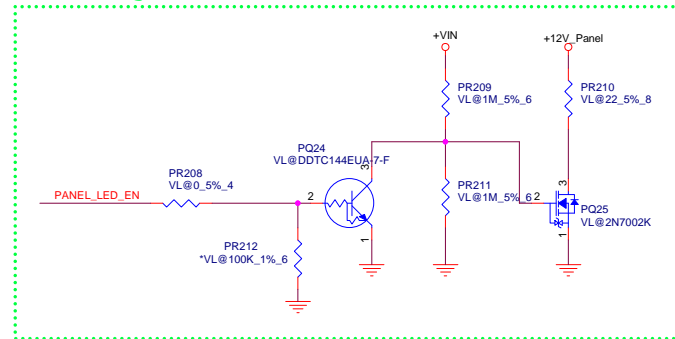


40V, 2A

VFB=1.238V

$$V_o = 1.238 * (1 + R1/R2) = 12V$$

BL Discharge Circuit

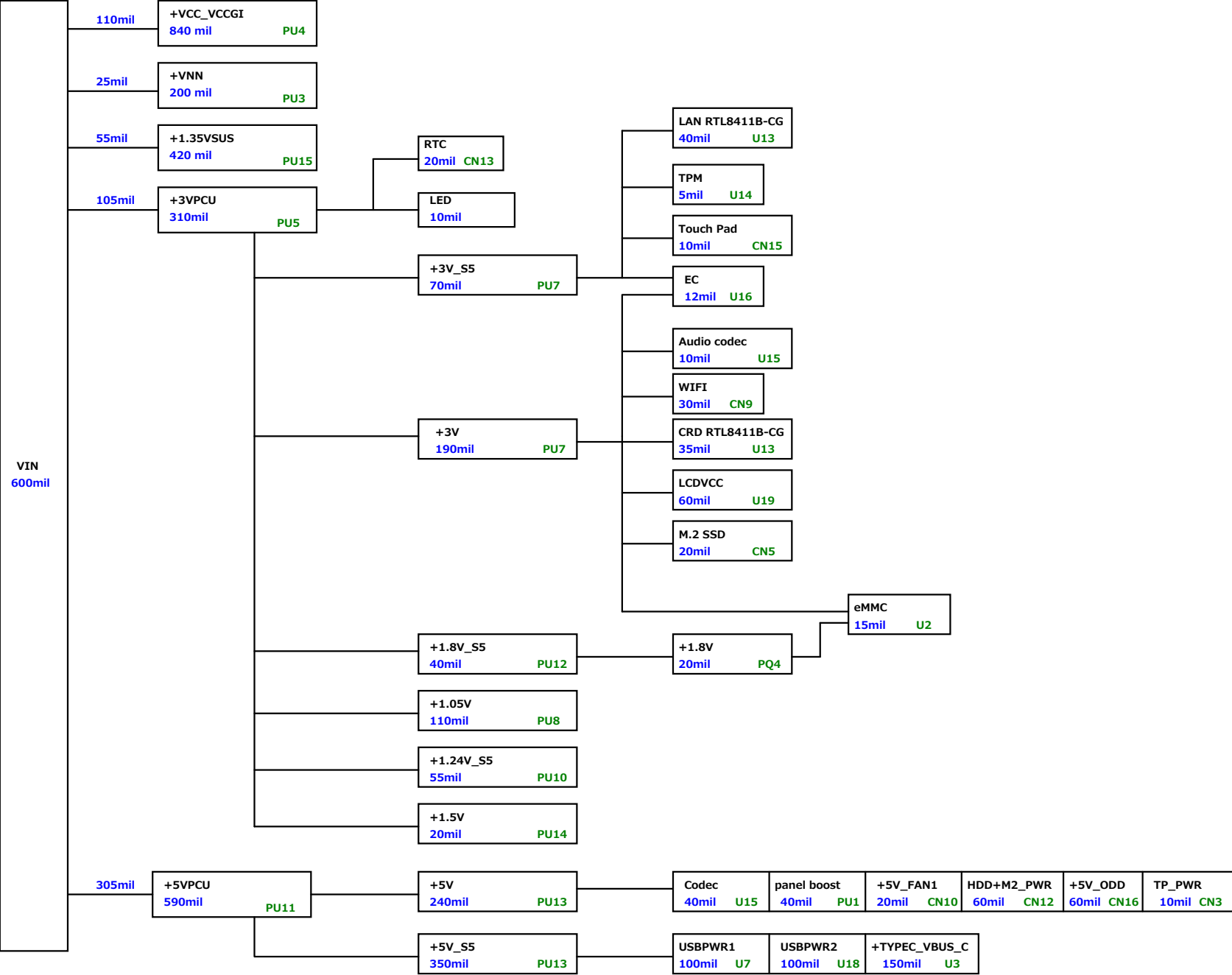


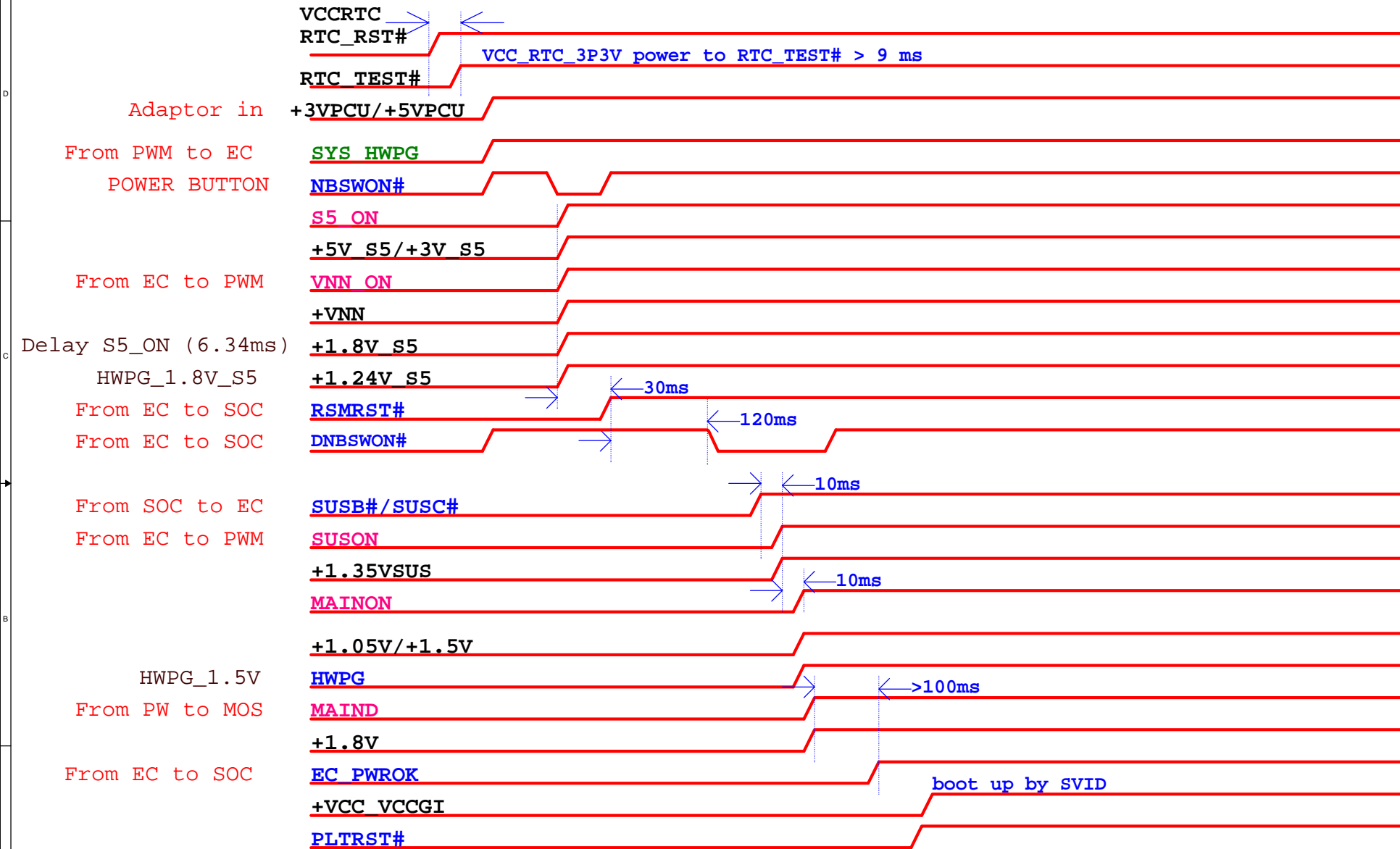
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PROJECT : ZAJ

LED Panel (TPS61087)

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Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF

Model	Date	CHANGE LIST
ZAJ REV.D	02/10	1.Remove U33/R482 2.Change 0 ohm to shortpad : R403,R404,R405,R406,R407,R408,R409,R410,R104,R113,R108,R115,R99,R402,R167,R165,R161,R158,R157,R153,R270,R271,R272,R273 3.Change C34 from 18pF to 15pF 4.Un-stuff R380/R464 (debug card circuit) 5.Change PR5/PR16 from 1% to 5%
	02/16	1.Remove HDMI EMI resistor -R131/R136/R141/R124
	02/18	1.Unstuff SW3 2.Update SW2 FP to "sw-ds-a40e-4p-smt" by SMT request 3.Update CN2 FP to "sdcard-156-1001902602-11p-smt" by SMT request 4.Update CN9 FP to "nglfl-apci0076-p001a-75p-ke-smt" by SMT request
	02/20	1.Un stuff PC211&PC212 then stuff PC203&PC194 by power team request 2.Un stuff PC107&PC112 then stuff PC121&PC122 by power team request 3.Change R158/R161 from shortpad to 0 ohm 4.Add C449&R493 for RSMRST#
	02/23	1.Modify Q31/Q33 from 2N7002 (Vgs=2.5V) to PJA138K (Vgs=1.5V) 2.Change CN14 QPN and FP to DFFC28FR029 -- "50584-0280n-v02-28p-l" by PDC request 3.Change CN17 QPN and FP to DFFC34FR026 -- "196332-34041-3-34p-l" by PDC request
Quanta Computer Inc.		
PROJECT MODEL: ZAJ		APPROVED BY:
DRAWING MODEL: ZAJ		DATE:
DRAWING BY:		REVISION: